Design Concepts for Semiconductor based Ultra-Linear Varactor Circuits (Invited)

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***Abstract* — For the implementation of RF tunable components, semiconductor based varactors provide advantages in terms of low control voltage, high capacitance density, low packaging costs, high reliability and technology compatibility. In this paper, an overview is given of the linearization approaches for semiconductor based ultra-linear varactors. Implementation issues regarding the optimum doping profiles are discussed. Design considerations for dedicated bias networks that provide optimum third-order intermodulation cancellation for the various varactor configurations are presented. To give an indication of the system-level responses for linear varactors, a varactor-based "true" time delay phase shifter is designed and the system-level linearity parameters, like adjacent channel power ratio (*ACPR*) and error vector magnitude (*EVM*), are evaluated for various application conditions.**

***Index Terms* — Adaptive systems, linear circuits, tunable circuits and devices, varactors.**

I. Introduction

With the introduction of more and more communication standards, tunable components, like capacitive switch banks and continuously tunable varactors, are considered to be enablers for truly generic transceivers that feature adjustable impedance, frequency and circuit transfer functions. Application examples include adaptive matching networks for multi-band/multi-mode power amplifiers, antenna mismatch correction networks, tunable filters, adjustable "true" time delay phase shifters, etc. For almost all these applications, linearity is one of the key parameters. This is especially true for applications in the densely populated wireless bands in the low GHz range. Initially, in order to address the need of very linear, low-loss tunable components, research has been focused on Micro Electro Mechanical Systems (MEMS) based solutions [1]-[7]. One popular implementation is the MEMS based capacitive switch bank [1]-[3]. However, its stringent requirement for a hermitic package and the relatively small capacitance density of MEMS, increases cost and form factor for applications below 10 GHz, especially when a large number of switching elements are required. In addition, the reliability of MEMS components still hampers their way to practical applications.

To overcome these disadvantages and establish suitable low-cost linear tunable components for applications below 10 GHz, research has been directed towards semiconductor based solutions. Examples are Silicon on Sapphire (SOS) / GaAs switches combined with MIM capacitor banks that act like switchable capacitors [8], [9], as well as continuously tunable ultra-low distortion Silicon-on-Glass (SOG) / GaAs varactors that make use of the third-order intermodulation (IM_3) cancelation techniques [10]-[18]. Although at first sight a switch based approach seems to be attractive in achieving high capacitance tuning ratios, the high voltage / linearity requirements in these applications demand extensive stacking of the switching components. This results in relatively high losses, which also tend to increase with the aimed resolution of the capacitive switch bank due to need of having multiple switching structures in parallel. These high losses disqualify this approach for the most demanding applications. In view of this, a varactor based approach can provide significantly higher quality factors while being continuously tunable. Over the last five years, various low-distortion varactor topologies have been proposed and experimentally verified within the TU Delft in-house silicon-on-glass (SOG) technology [11]-[17] as well as in Skyworks' preproduction GaAs technology [18]. In these works, superior linearity has been demonstrated for the semiconductor based varactors. In this paper, we review the linearization approaches for these semiconductor based varactors together with their optimum doping profiles, and investigate their "system-level" response to modern communication signals with different bandwidth or data rate.

II. Semiconductor Based Ultra-Linear Varactor Circuits

A. Ultra-Linear Varactor Configurations

Conventional semiconductor based varactors, like the p-n diode, Schottky diode and MOS varactors, are continuously tunable voltage-controlled capacitances,

TABLE I REQUIRED CONDITIONS FOR IM_3 CANCELLATION AND THE RESULTING LINEARITY PRODUCTS FOR DIFFERENT SEMICONDUCTOR VARACTOR CONFIGURATIONS

	single diode [classic $C(V_R)$]	**distortion-free varactor stack (DFVS)**	**high tuning range varactor stack (HTRVS)**	**single diode [exponential $C(V_R)$]**	**narrow tone-spacing varactor stack (NTSVS)**	**wide tone-spacing varactor stack (WTSVS)**
$C(V_R)$ relation	$C_{j0}\left(1+\frac{V_R}{V_j}\right)^{-n}$ ($V_R > 0$, $V_j > 0$)	$C_{j0}\left(1+\frac{V_R}{V_j}\right)^{-0.5}$	$C_{j0}\left(1+\frac{V_R}{V_j}\right)^{-n}$ ($n > 0.5$)	$C_{j0}\exp(-a_2 V_R)$	$C_{j0}\exp(-a_2 V_R)$	$C_{j0}\exp(-a_2 V_R)$
Topology	single [Fig. 1(a)]	anti-series [Fig. 1(b)]	anti-series/ anti-parallel [Fig. 1(c)]	single [Fig. 1(a)]	anti-series [Fig. 1(b)]	anti-series/ anti-parallel [Fig. 1(c)]
Center-tap impedance [$Z_c(s)$]	no center-tap impedance	infinity for all frequencies	infinity for all frequencies	no center-tap impedance	zero at low frequency infinity at other frequencies	infinity for all frequencies
Area ratio for IM_3 cancellation	no cancellation	1:1	$X=\frac{4n+1+\sqrt{12n^2-3}}{2(n+1)}$	no cancellation	1:1	$X=2\pm\sqrt{3}$
IP_2	at f_1+f_2 $\frac{V_R+V_j}{n}$	for all even-order mixing ∞	for all even-order mixing ∞	at f_1+f_2 $\frac{1}{a_2}$	for all even-order mixing ∞	for all even-order mixing ∞
IP_3 at $2f_1$-f_2	$\frac{2\sqrt{2}\left(V_R+V_j\right)}{\sqrt{n(n+1)}}$	for large Δf ∞	for large Δf ∞	$\frac{2\sqrt{2}}{a_2}$	for small Δf ∞	for large Δf ∞
IP_4	at f_1+f_2 $\frac{\sqrt[3]{4}\left(V_R+V_j\right)}{\sqrt[3]{n(n+1)(n+2)}}$	for all even-order mixing ∞	for all even-order mixing ∞	at f_1+f_2 $\frac{\sqrt[3]{4}}{a_2}$	for all even-order mixing ∞	for all even-order mixing ∞
IP_5 at $2f_1$-f_2	$\frac{2\sqrt{6}\left(V_R+V_j\right)}{\sqrt[4]{15n(n+1)(n+2)(n+3)}}$	for large Δf ∞	for large Δf $2.72\left(V_R+V_j\right)$ ($n = 1$, $X = 2$)	$\frac{2\sqrt{6}}{\sqrt[4]{15}a_2}$	for small Δf $\frac{3.52}{a_2}$	for large Δf $\frac{2.75}{a_2}$

Symbols: C_{j0} is the capacitance at zero bias; V_j is the built-in voltage; V_R is the reverse control voltage; a_2 is the capacitance grading coefficient [14]; n is capacitance power law coefficient [19]; Δf is the frequency difference or tone spacing of two-tone input RF signals; IP_2, IP_3, IP_4 and IP_5 are the second-order, third-order, fourth-order, and fifth-order voltage interception point respectively.

which make use of the variable depletion layer thickness around the junction. These devices show advantages in terms of capacitance density, integration, reliability, tuning speed (1-100 ns), low control voltage and ruggedness. However, their inherently nonlinear behavior is normally considered to be incompatible with the linearity requirements of modern wireless communication systems. To improve the linearity, recently, several specific varactor diode topologies have been developed and implemented [11]-[18]. These proposed varactor configurations act as variable capacitors between their RF terminals with ideally zero, or extremely low distortion, while a third terminal is used for a "low-frequency" control voltage. A brief description of these low-distortion varactor configurations is given below.

- The distortion-free varactor stack (DFVS) [11], [13] is based on an anti-series connection of two identical uniformly doped diodes [Fig. 1(b)]. This uniform doping results in a capacitance power law coefficient of $n=0.5$ [19]. Furthermore, an "infinitely" high impedance is used to connect to the center-tap termination. Under these conditions, all distortion components at the RF terminals are perfectly cancelled, yielding distortion-free device operation for RF signals.
- The high-tuning range varactor stack (HTRVS) [11] is a combined anti-series/anti-parallel topology of four hyperabrupt varactor diodes [Fig. 1(c)] [19]. Now a capacitance power law coefficient $n>0.5$ is applied along with two "infinitely" high center-tap impedances. At the RF

terminals, the resulting even and third-order distortion products are cancelled through a proper selection of the varactor area ratio (*X)*

$$X = \frac{4n+1+\sqrt{12n^2-3}}{2(n+1)}. \quad (1)$$

- The narrow tone-spacing varactor stack (NTSVS) [14]-[16], [18] is based on an anti-series connection of two $N_d x^{-2}$ doped diodes [Fig. 1(b)], with N_d being the maximum doping concentration and x the depth. Note that this special doping profile results in exponential $C(V_R)$ behavior under a reverse bias voltage (V_R). To cancel the third-order intermodulation distortion (IM_3), there must be a *low impedance* path (relative to the AC impedance of the varactor capacitance itself) between the center node [node c in Fig. 1(b)] and the two RF terminals at low frequencies. At the same time, the high-frequency components (fundamental and higher harmonics) at the center-tap node should experience high impedance, i.e., $Z_c(s)$ should be much larger than the AC impedance of the varactor diode itself at these frequencies. When these conditions are met, the IM_3 will be cancelled and the remaining distortion is dominated by the much smaller fifth-order nonlinearity.
- The wide tone-spacing varactor stack (WTSVS) [15] is a combined anti-series/anti-parallel topology of four $N_d x^{-2}$ doped diodes, which uses an "infinitely" high impedance as center-tap connection [Fig. 1(c)]. This situation can be regarded as a special case of the HTRVS in which the capacitance power law coefficient n approaches infinity. This yields a corresponding varactor area ratio for IM_3 cancelation of $2 \pm \sqrt{3}$. Note that this configuration shares the same doping profile as the NTSVS and therefore both configurations (WTSVS and NTSVS) can be implemented on the same wafer while offering complementary linearity properties in terms of tone spacing.

In Table I, the conditions required for IM_3 cancellation and the resulting linearity products, i.e., second-order intercept point (IP_2), IP_3, IP_4 and IP_5, are summarized and compared for different varactor configurations. A physics based circuit simulation library is available at [20]. Generally speaking, the varactor configurations that use "infinitely" high center-tap impedance(s) (i.e., DFVS, HTRVS and WTSVS) provide the best linearity for signals that have a relatively wide frequency spacing (larger than several hundred kilohertz), whereas the NTSVS provides the highest linearity for signals with a relatively narrow frequency spacing (up to ten's of MHz). The fact that the latter configuration (NTSVS) makes use of a base-band "short" for the connection to the center-tap termination facilitates rapid modulation of its tunable capacitance, something that is beneficial for future RF applications like dynamic load-line power amplifiers or modulators.

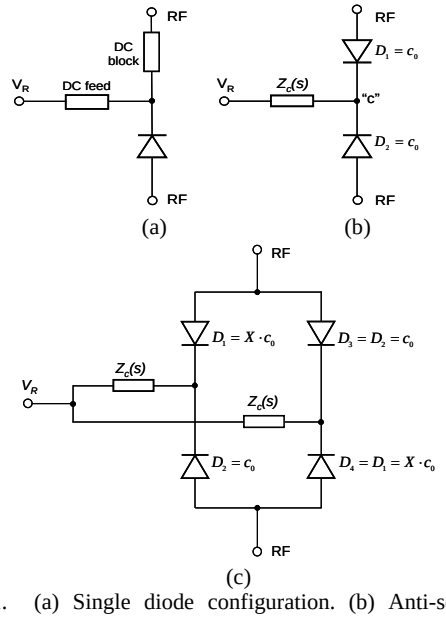


Fig. 1. (a) Single diode configuration. (b) Anti-series configuration for DFVS and NTSVS. (c) Anti-series/anti-parallel configuration for HTRVS and WTSVS.

B. Optimum Doping Profiles for Varactor Diodes

In order to achieve the capacitance power law coefficient n = 0.5 for the DFVS, a uniform doping profile is required as shown Fig. 2(a). This doping concentration needs to be chosen carefully since this sets the quality factor and device breakdown. When the desired tuning range is known, i.e., $T_{tune} = C_{max}/C_{min}$ with C_{max} and C_{min} being the maximum and minimum capacitance values, together with the material parameters, like maximum electric field ($E_{breakdown}$), dielectric constant (ε_s), mobility (μ_n) and built-in potential (V_j), the best possible choice for the doping concentration ($N_{uniform}$) can be selected using

$$N_{uniform} = \frac{\varepsilon_s E^2_{breakdown}}{2eV_j(T^2_{tune}-1)}, \quad (2)$$

where e is the electron charge. With this selection, the related highest achievable intrinsic quality factor for the varactor at zero bias (Q_{opt}) operation is defined as

$$Q_{uniform}\Big|_{V_R=0} = \frac{\mu_n E^2_{breakdown}}{2\omega V_j(T^2_{tune}-1)(T_{tune}-1)}, \quad (3)$$

where ω is the angular RF frequency [17].

For the NTSVS and WTSVS, the required $N_d x^{-2}$ doping profile, which provides the exponential $C(V_R)$ relationship, is shown in Fig. 2(b). Since we cannot implement infinitely high or extremely low doping concentrations, the $N_d x^{-2}$ relationship is restricted between x_{low} and x_{high}, which automatically defines the useful capacitance tuning range. To maintain the "exponential" $C(V_R)$ relation and avoid reducing the

breakdown voltage and quality factor, a lowly doped spacer layer [Region 1 in Fig. 2(b)] is required. The resulting doping profile and maximum achievable intrinsic quality factors at zero bias for these structures can be written as [17]

$$N(x) = \frac{\varepsilon_s V_{R\_\max}}{e \ln(T_{tune})} x^{-2}, \quad (4)$$

$$Q\Big|_{V_R=0} = \frac{3\mu_n \ln(T_{tune})}{\omega V_{R\_\max}(T_{tune}^3 - 1)} \left(\frac{T_{tune} E_{breakdown}}{T_{tune} - 1} \right)^2. \quad (5)$$

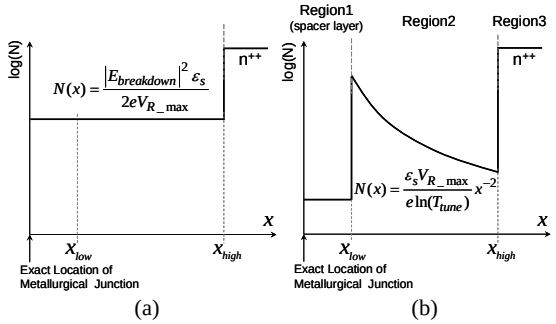


Fig. 2. (a) Optimized doping profile of the uniform doped diode for the DFVS. (b) Optimized doping profile for the NTSVS and WTSVS to achieve the exponential $C(V_R)$ relation.

C. Optimum Design of the Center-tap Networks

It is important to note that the frequency spacing region where the IM_3 is cancelled is strongly dependent on the center-tap networks [$Z_c(s)$], and for this reason, we discuss here the design considerations of various center-tap networks for the different varactor configurations.

For the varactor configurations that make use of an "infinitely" high center-tap impedance, the IM_3 cancellation requires that the center-tap impedance must be much higher than the AC impedance offered by the varactors themselves. This requirement is difficult to fulfill for the baseband frequency component of a two-tone signal (f_2-f_1) when the tone spacing approaches zero, since for the related baseband frequency the capacitive reactance of the varactors increases without bound. Consequently, there is a lower frequency limit of tone spacing where the third-order distortion cancellation is violated. In practical implementations, an integrated resistor can be used for the dc biasing networks at the center-tap termination. Moreover, a pair of anti-parallel diodes as shown in Fig. 3 can be added to provide very high impedance extending the high linearity operation region to very low tone spacing.

In view of this, the simulated and measured distortion components at $2f_1$-f_2 of the DFVS are depicted in Fig. 4 as function of tone spacing (f_2-f_1) at a power of 18 dBm per tone [13]. In this experiment, the IM_3 cancellation starts to work above 100 kHz for the DFVS with 80-kΩ center-tap resistor, while when the center-tap connection of the DFVS is composed of an 80-kΩ resistor combined with a pair of anti-parallel diodes, the workable IM_3 cancellation region is extended to a much lower tone spacing.

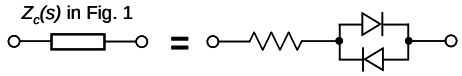


Fig. 3. The combination of a resistor and anti-parallel diodes used as $Z_c(s)$ [see Fig. 1(b) and (c)] for linearity improvement at low tone spacing for varactor configurations that make use of an "infinitely" high center-tap impedance.

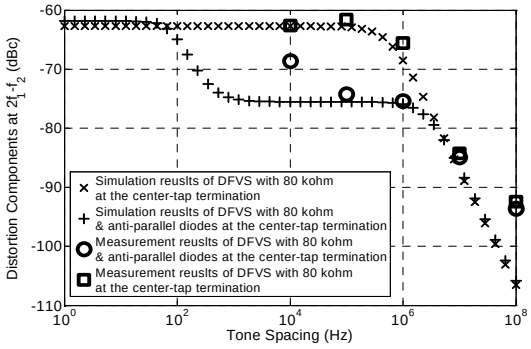


Fig. 4. Simulated and measured distortion component at $2f_2$-f_1 as function of tone spacing at a power level of 18 dBm for the DFVS making use of TU Delft in-house silicon-on-glass technology (f_{center} = 2.14 GHz, V_R = 5 V and C_{j0}=2.3 pF) [13].

In contrast to the varactor configurations that use "infinitely" high center-tap impedance, the NTSVS requires zero center-tap impedance for the baseband frequencies and "infinitely" high impedance for the fundamental and all higher harmonic frequencies. Note that this center-tap impedance requirement is relative to the impedance offered by the varactor capacitance itself at these frequencies. In practical implementations, this can be a single resistor or an inductor, since the capacitive reactance of the varactor stack itself exhibits relatively high impedance at low tone spacing. To understand this point, in Fig. 5 the magnitude of the impedance is plotted as function of frequency for a 5-pF capacitor, a 2-kΩ resistor and a 10-nH inductor. It can be observed that both 2-kΩ resistor and 10-nH inductor provide relatively large impedance at 2 GHz (e.g. as a rule of thumb, 10× larger than offered by the 5-pF capacitor), whereas the baseband "short" requirement for the NTSVS (e.g. as a rule of thumb, typically 25× smaller impedance than that varactor), is valid up to 300 kHz for the 2-kΩ resistor and up to 70 MHz for the 10-nH inductor. A more advanced center-tap impedance network, like the topology shown in Fig. 6, can be used to further extend the valid frequency region for a baseband "short". The combination of capacitor and inductor shown in Fig. 6, forms a series resonator around 150 MHz, while the 100-Ω shunt

resistor provides the baseband "short" condition for lower frequencies. As a result, the frequency region where the baseband "short" approximation is valid can be extended up to 180 MHz.

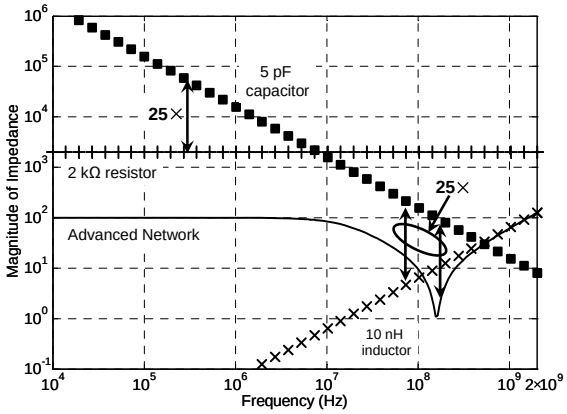


Fig. 5. The impedance magnitude as function of frequency for a 5-pF capacitor, a 10-nH inductor, a 2-kΩ resistor and a more advanced center-tap network (see Fig. 6).

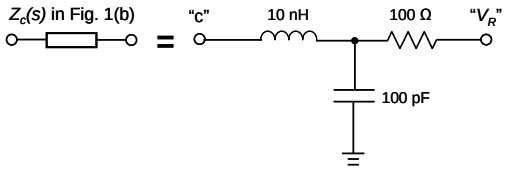


Fig. 6. NTSVS center-tap network that provides an extended bandwidth for the baseband "short" condition relative to the impedance of the varactor.

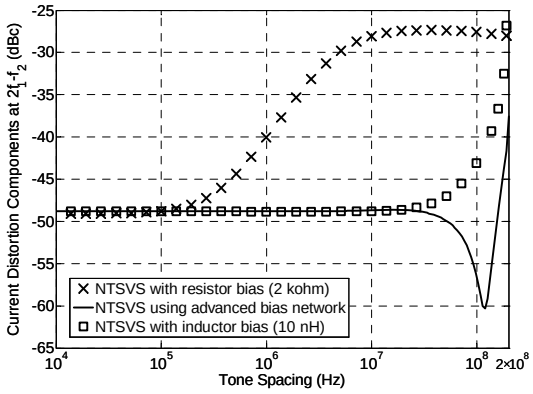


Fig. 7. Simulated capacitive current distortion component at $2f_1$-f_2 versus the tone spacing of the input RF voltage signal (a_2=0.183 V^{-1} , V_{R_max}=12 V, V_R=5 V, V_{RF_peak}=10 V, f_{RF_center}=2 GHz and effective capacitance at zero bias=10 pF) for the NTSVS with different center-tap networks.

Fig. 7 shows the simulated two-tone linearity as the dBc ratio of the fundamental and distortion current (at $2f_1$-f_2) versus tone spacing of the RF input signal. As expected, the NTSVS behaves linear at narrow tone spacing and less linear for very large tone spacing. More precisely the linearity of the NTSVS with 2-kΩ center-tap resistor and 10-nH center-tap inductor start to degrade at 300 kHz and 70 MHz respectively, while excellent linearity can be ensured up to ~180 MHz for a NTSVS with a more advanced center-tap network.

As experimental evidence, four test structures have been fabricated within Skyworks' GaAs technology, namely: a 10-pF GaAs NTSVS with 10-nH inductive center-tap connection; a 10-pF GaAs NTSVS with 2-kΩ resistive center-tap connection; a 2.5-pF GaAs NTSVS with 10-kΩ resistive center-tap connection and a 10-pF GaAs WTSVS with 200-kΩ resistive center-tap connection. The measured capacitance tuning range of these varactor diodes is 9:1 with a maximum control voltage of 12 V [18]. Linearity testing was performed using a two-tone signal (f_{center}=2 GHz) with varying tone spacing making use of an active load-pull system [21]. The measured distortion component at $2f_2$-f_1 is plotted as function of tone spacing for an output power level of 20 dBm in Fig. 8. It can be concluded from Fig. 8 that the linearity of the resistive center-tapped NTSVS degrades around a few hundred kilohertz while the inductive center-tapped NTSVS can preserve a good linearity up to ten's of MHz. It can be also observed that the WTSVS and the NTSVS, which both feature the $N_d x^{-2}$ doping profile for their varactor diodes, have complementary linearity behavior in terms of tone spacing. This facilitates to address the different linearity requirement of RF adaptive systems in one single technology [15].

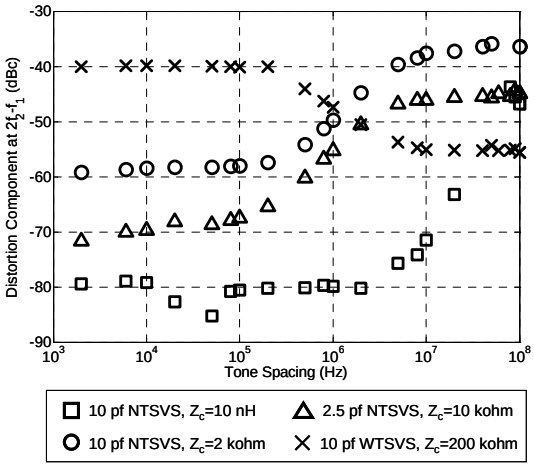


Fig. 8. Measured distortion component at $2f_2$-f_1 as function of tone spacing at a power level of 20 dBm for the WTSVS and NTSVS making use of Skyworks' GaAs technology (for all cases: f_{center} = 2 GHz, a_2 = 0.183 V^{-1} and V_R = 5 V).

III. System Level Linearity Performance

At the circuit level, the linearity of the varactors can be evaluated by monitoring the intermodulation product of a two-tone signal (i.e., IM_3 or IM_5) while varying its tone spacing. When considering the linearity performance of a communication system with a given channel bandwidth, intermodulation distortion will give rise to in-band and out-of-band interference. Out-of-band interference will disturb the

information detection of the adjacent-channel users, while the in-band intermodulation products that fall within the assigned transmit bandwidth will pollute the transmitted information by changing its original constellation points, causing difficulties in signal detection. To study these effects, industry uses the adjacent channel power ratio (*ACPR*) to evaluate the out-of-band interference and the error vector magnitude (*EVM*) as a figure of merit describing how the transmitted information becomes distorted.

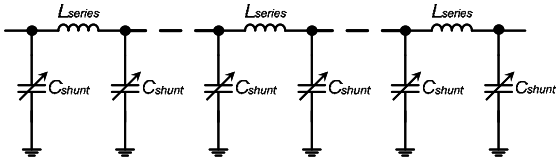
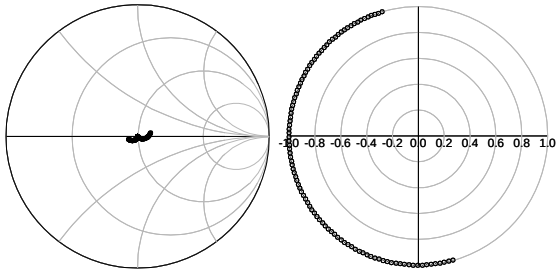


Fig. 9. Schematic of the true-time-delay phase shifter to be used for system-level linearity comparison for different varactor configurations. [To achieve a phase shift of 180°, eight ∏ low-pass sections are cascaded. The lossless series inductances (L_{series}) are fixed as 0.36 nH, while the shunt capacitances (C_{shunt}) are tuned from 7.35 pF to 13.60 pF. The characteristic impedance is 5 Ω.]

In this section, we investigate the system-level response of the linear varactor configurations under different bandwidth or data-rate conditions. For this purpose, as a practical application of linear varactors, a varactor-based phase shifter is created as shown in Fig. 9. This true-time-delay type 180° phase shifter is composed of eight cascaded ∏ low-pass sections, of which the lossless series inductances (L_{series}) are fixed as 0.36 nH, while the shunt capacitances (C_{shunt}) can be tuned from 7.35 pF to 13.60 pF. The simulated s_{11} and s_{21} are given in Fig. 10, showing a good matching at the input while providing a phase control of 180°.



(a) (b)

Fig. 10. (a) The simulated s_{11} of the fictive phase shifter (b) Polar plot of the simulated s_{21}. [The lossless series inductances (L_{series}) in Fig. 9 are fixed as 0.36 nH, while the shunt capacitances (C_{shunt}) are tuned from 7.35 pF to 13.60 pF. The characteristic impedance is 5 Ω and the RF frequency is 2 GHz].

In practice, the tunable shunt capacitors (C_{shunt}) can be implemented by different varactor configurations to compare their linearity behavior, i.e., (i) varactor stack with an exponential C-V_R relation but with incorrect harmonic terminations, (ii) narrow tone-spacing varactor stack (NTSVS) with 5-nH center-tap inductance, (iii) distortion-free varactor stack (DFVS) with 100-kΩ center-tap resistance, (iv) DFVS with 1-MΩ center-tap resistance. In order to handle peak power up to 40 dBm while avoiding very high voltage swings over the varactor diodes, the characteristic impedance of the phase shifter is set to 5 Ω. Consequently, for the implementation using the DFVS, the control voltage needs to be tuned from 4 V to 12 V to obtain an effective capacitance tuning range of 1.85 for this peak power. Accordingly, the grading coefficient (a_2) of those varactor diodes with an exponential C-V_R relation is normalized as 0.0528 V^{-1} to maintain the same effective tuning range over the given voltage range.

To study the linearity of the phase shifter, of which the tunable capacitances (C_{shunt}) are implemented using the different varactor configurations, the circuit is first simulated using a two-tone signal. For our test we select the worst case condition, i.e., the peak power level equals 40 dBm for each tone, while varying the tone spacing (Fig. 11). It can be observed that the phase shifter that makes use of DFVS starts to offer better linearity than the varactor stack (with incorrect harmonic terminations) above 1 kHz for the center-tap resistance of 1 MΩ and above 10 kHz for the center-tap resistance of 100 kΩ, while the phase shifter implemented with the NTSVS provides superior linearity up to 30 MHz.

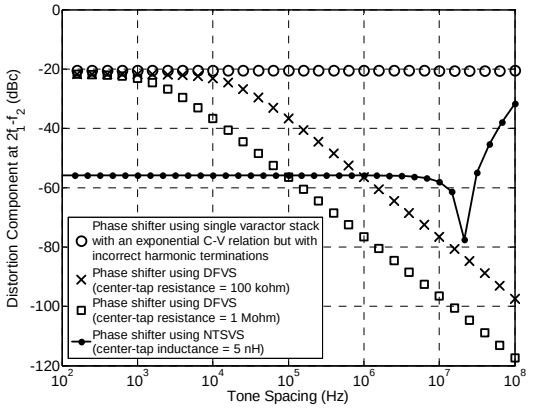


Fig. 11. Simulated distortion components for the 180° phase shifter at $2f_1$-f_2 in dBc with respect to the fundamental power (40 dBm each tone) as a function of the tone spacing of the RF input signal. The tunable capacitances (C_{shunt}) are implemented using different varactor configurations, i.e., (i) varactor stack with an exponential C-V_R relation but with incorrect harmonic terminations, (ii) NTSVS with 5-nH center-tap inductance, (iii) DFVS with 100-kΩ center-tap resistance, (iv) DFVS with 1-MΩ center-tap resistance. The diode parameters are: a_1 = 33.90 pF and a_2 = 0.0528 V^{-1} for the varactor stack with incorrect harmonic terminations; a_1 = 34.45 pF and a_2 = 0.0528 V^{-1} for the NTSVS; C_{j0} = 78.2 pF and V_j = 0.7 V for the DFVS. The RF frequency is 2 GHz, while the applied reverse bias (V_R) is 10 V in all situations.

For the system-level linearity comparison, we consider the schematic as shown in Fig. 12. A relatively spectrally pure quadrature phase-shift keying (QPSK) signal with a mean power of 35 dBm and the peak-to-average ratio of 4.35 dB is used as the signal source (see the input signal in Fig. 12), of

which the bandwidth and data rate can be adjusted for different applications. Here, as listed in Table II, we study two cases: the moderate data-rate application with the symbol rate of 135.5 kHz and the high data-rate application with symbol rate of 3.6864 MHz.

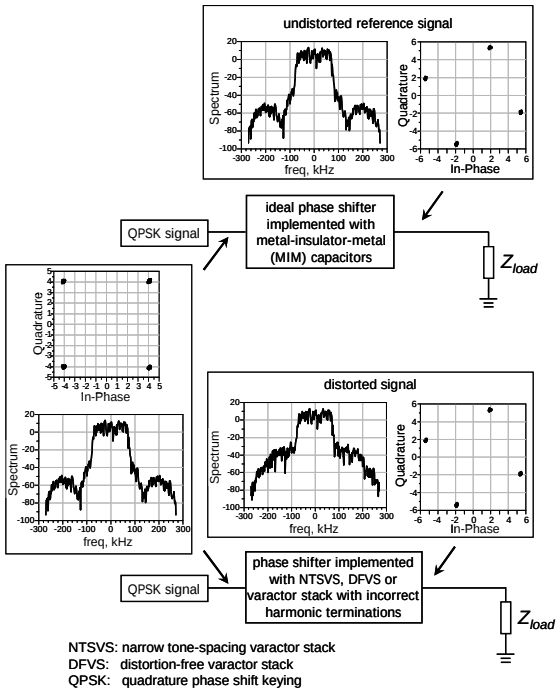


Fig. 12. Schematic for the linearity comparison of the phase shifter. Note that nonlinear tunable components are used in this figure to generate the distorted output signal.

TABLE II PARAMETERS USED FOR THE SYSTEM-LEVEL LINEARITY COMPARISON

	bandwidth	symbol rate	integration region for *ACPR* calculation (offset frequency)
high data-rate application	5 MHz	3.68 MHz	-6.84 MHz~-1.84 MHz 1.84 MHz~6.84 MHz
moderate data-rate application	200 kHz	135.5 kHz	-300 kHz ~ -100 kHz 100 kHz ~ 300 kHz

Since *EVM* is a figure of merit describing how the constellation points are shifted from their original places during transmission, it is important to note that the "ideal" phase shifter structure itself, as well as the nonlinearities of the varactors used in such a phase shifter, will change the positions of the constellation points of the transmit signal. Fortunately, a true-time delay phase shifter only rotates constellation points without distorting the signal. In Fig. 12, a reference phase shifter path, of which the shunt capacitance (C_{shunt} in Fig. 9) is implemented with perfectly linear metal-insulator-metal (MIM) capacitors, is used to normalize the rotation of the constellation points. By doing so, when comparing the degradation of the *EVM* of the phase shifters, this degradation can be totally assigned by the distortion contributions of the varactors. In the meanwhile, the *ACPR* of the distorted signal and the undistorted reference signal can be tested and compared.

The simulated *EVM* and *ACPR* for the moderate and high data-rate applications are listed in Table III. It can be observed that the *EVM* and *ACPR* of the varactor stack with incorrect harmonic terminations are the worst for both application cases, as reflected by the IM_3 products of -20 dBc over the whole range of the tone spacing up to 100 MHz (Fig. 11). On the other hand, the simulated *EVM* and *ACPR* of the NTSVS are extremely small for both application cases, which means the NTSVS raises neither in-band nor out-band distortion. These results agree very well with the two-tone results in Fig. 11, where the NTSVS provided a superior linearity up to 30 MHz. For the DFVS, as shown in Fig. 11, it starts to provide better linearity above 1 kHz for the center-tap resistance of 1 MΩ and above 10 kHz for the center-tap resistance of 100 kΩ. Since the bandwidths under consideration are both at least 10 times larger than the tone spacing where the DFVS behaves nonlinear, the linearity performance evaluated by *ACPR* survives for both application cases. However, the *EVM* results reveal that the DFVS topology raises in-band distortion for the moderate data-rate application and this can be explained by its linearity limitations at low tone spacing as earlier indicated in Fig. 11. In summary, it can be concluded for this application oriented example that the NTSVS is suitable for both moderate and high data-rate applications, while the DFVS may raise some in-band distortion when the bandwidth under consideration is relatively small. It is important to note that the system-level linearity performance can be well explained by the two-tone circuit-level linearity results, a property that allows one to select the most proper varactor configurations for a given application.

V. CONCLUSION

In this paper, various low-distortion semiconductor-based varactor topologies have been reviewed and compared. Design issues regarding the doping profile for quality factor optimization as well as the implementation of the center-tap connections for the third-order intermodulation cancellation have been discussed for different varactor configurations. As a practical application example, a varactor-based phase shifter is designed and used to investigate the system-level responses of the linear varactor configurations under different bandwidth or data-rate conditions. It confirms that different center-tap connections have a strong impact on the system linearity. It also turns out that this linearity performance can be well explained by comparing

TABLE III SIMULATED ACPR AND EVM FOR HIGH AND MODERATE DATA-RATE APPLICATIONS

	high data-rate application (symbol rate = 3.6864 MHz)			**moderate data-rate application (symbol rate = 135.5 kHz)**		
	ACPR (dBc)		*EVM* relative to the undistorted reference (%)	*ACPR* (dBc)		*EVM* relative to the undistorted reference (%)
	lower sideband	upper sideband		lower sideband	upper sideband	
undistorted reference (MIM capacitor)	-63.44	-63.54	0	-58.46	-58.90	0
NTSVS $Z_c(s)$ =5 nH	-63.42	-63.50	0.008	-58.36	-58.93	0.002
varactor stack with incorrect terminations	-46.18	-45.08	0.256	-43.84	-43.99	0.253
DFVS $Z_c(s)$ = 100 kΩ	-63.43	-63.52	0.054	-58.03	-56.25	0.439
DFVS $Z_c(s)$ = 1 MΩ	-63.44	-63.54	0.013	-58.67	-59.01	0.113

with two-tone simulations, a property that can be used as a reference to select the most proper varactor configurations for a given application.

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